IIT 2018 School, September 13-15, 2018

- Program
- Abstracts of the Lectures
- Resumes of the Lecturers

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James Ziegler

Wednesday, Sept. 12	
16:00 – 20:00	Registration
18:00	Welcome Reception

Ion Implantation Background

Thursday, Sept. 13	Subject	Speaker
9:00 – 10:30	History of Integrated Circuits and Ion Implantation	James Ziegler
10:30 – 11:00	Coffee	
11:00 – 12:00	Ion Implantation: Current and Future CMOS ICs	Leonard Rubin
12:00 – 13:30	Lunch	
13:30 – 15:00	Recent and Current Status of Ion Implantation Systems	Michael Current
15:00 – 15:30	Coffee	
15:30 – 17:00	Analytic Techniques for Ion Implantation	Dick James

Ion Implantation Equipment
(Parallel Session)

Friday, Sept. 14	Subject	Speaker
9:00 – 10:30	Ion Implantation Systems	Bo Vanderberg
10:30 – 11:00	Coffee	
11:00 – 12:00	Source Physics and Maintenance	Anthony Renau
12:00 – 13:30	Lunch	
13:30 – 15:00	Safety Considerations in Ion Implantation	Ewald Wiltsche
15:00 – 15:30	Coffee	
15:30 – 17:00	Ion Beam Purity and Elemental Contamination	Michael Current

Implantation Science
(Parallel Session)

Friday, Sept. 14	Subject	Speaker
9:00 – 10:30	Ion Implantation Damage	Kevin Jones
10:30 – 11:00	Coffee	
11:00 – 12:00	Ion Implantation Annealing	Kevin Jones
12:00 – 13:30	Lunch	
13:30 – 15:00	Annealing for Si, Ge, SiC, and GaN	Wilfried Lerch
15:00 – 15:30	Coffee	
15:30 – 17:00	Cluster Ion Beams: History and Technology	Jiro Matsuo

Future Applications

Saturday, Sept. 15	Subject	Speaker
9:00 – 10:00	Advanced Ion Implant Concepts	Leonard Rubin
10:00 – 11:00	Ion Implantation in Power Devices, new Base Materials, and Solar Cells	Werner Schustereder
11:00 – 11:30	Coffee	
11:30 – 13:00	High Performance CMOS: 7 nm & Beyond	Devendra Sadana
13:00	End of School	

Abstracts of the Lectures:

History of Integrated Circuits and Ion Implantation (James Ziegler)

Ion Implantation was the critical innovation that catalyzed the integrated circuit industry in 1975-1977 to its exponential growth in the following two decades. This history reviews the landmarks of solid-state electronics, showing its slow growth with an expansion of about 10% per year for its first 70 years. Suddenly, three ion implantation innovations came together in the early 1970's that reduced the costs associated with integrated circuit manufacturing by 70%. This led immediately to new microprocessors (and the PC), micro-controllers for autos and machinery, and large scale memory chips for complex software.

Ion Implantation: Current and Future CMOS ICs (Leonard Rubin)

The flexibility of ion implantation in the selection of dopant species, spatial location within the device, and subtle concentration profile control enables rapid introduction of new integrated process technologies, and precise optimization or elimination of performance tradeoffs in circuit technologies. Ion implantation is essential to the fabrication of advanced devices. This presentation will review the history, function, and future trends of traditional and emerging applications of ion implantation in CMOS devices, including both doping and non-doping (material modification) implants. Ion implant applications for both planar and three dimensional (FinFET) transistors will be discussed.

Commercial Ion Implantation Systems (Michael Current)

Ion implantation processing of electronic materials and devices use a wide variety of accelerator systems and end stations as well as many special techniques. After a concise outline of the basics of accelerator components (ions sources, ion selection, acceleration, scanning, charge control and dosimetry), examples of the major types of commercial ion implantation systems for medium and high current, high energy, plasma immersion as well as special tools for doping of large-area flat-panels and photo-voltaic cells will be reviewed. Each example system will be described in a tutorial fashion for its component layout, accelerator and beam/wafer scanning mechanisms, performance characteristics in terms of ion energy range and beam current and special capabilities

Analytic Techniques for Ion Implantation (Dick James)

Ion implants result in structural, electronic, and chemical modifications to the implanted material. This session will discuss the different methods available to examine and characterize those changes, ranging from imaging techniques such as transmission electron microscopy (TEM) to more quantitative procedures such as secondary ion mass spectrometry (SIMS).

Ion Implantation Damage (Kevin Jones)

This talk will explore the origin of radiation damage that occurs during ion implantation of silicon. The talk will discuss the formation of point defects and the amorphization of Si by both dopant and non-dopant ions.

Ion Implantation Annealing (Kevin Jones)

This talk will discuss the processes that occur during the annealing of an implanted Si layer. This includes the crystallization of any implantation induced amorphous layers as well as the evolution of excess point defects upon annealing and their effect on junction formation.

New Advancements in Ion Implantation Annealing for Si, Ge, SiC, and GaN (Wilfried Lerch)

Thermal processes are some of the key steps in semiconductor manufacturing. A critical issue associated with the continuous reduction of dimensions of CMOS transistors is the realization of highly conductive, ultra-shallow junctions for source/drain extensions. The temperature-time cycle has changed radically over the past 10 years. Lamp-based thermal annealing, for a period of seconds, evolved to spike anneals of one second and then to flash-lamp annealing or laser annealing. These provide an ultra-sharp temperature peak of the order of ms and are favoured for this kind of activation anneals. This talk reviews various annealing equipment and their annealing schemes (temperature-time cycles and gaseous ambient) and investigates the formation of ultra-shallow, highly-electrically-activated and custom-shaped junctions. Moreover, annealing of defects is always combined to the activation anneal therefore the deactivation of highly-activated junctions will be reviewed. Furthermore the activation techniques in the diamond-like semiconductor Germanium and in the wide-band-gap ones, SiC and GaN, are discussed in detail.

Cluster Ion Beams: History and Technology (Jiro Matsuo)

Reviews the development of cluster ion beam technology, including the brief history, fundamental characteristics of cluster ion to solid surface interactions, emerging industrial applications, and identification of some of the significant events which occurred as the technology has evolved into what it is today. The new ion beam processes, using cluster ions which consist of substantial numbers of atoms or molecules, are very different from those produced by impact of conventional ions comprised of single atoms or molecule. Cluster-surface collisions produce important non-linear effects which are being applied to shallow junction formation, to etching and smoothing of semiconductors, metals, and dielectrics, to assisted formation of thin films with nano-scale accuracy, and to other surface modification applications.

Ion Implantation Systems (Bo Vanderberg)

In this lecture, we will review modern ion implanters for semiconductor applications across the entire application space: high current, medium current and high energy. First, concepts fundamental to implanter beamline technology will be examined: ion beam generation, including ion sources and extraction; and transport, including acceleration, focusing and filtering, such as mass analysis. These concepts will be illustrated with exemplary beamline elements used in modern equipment. We will then cover the ion implantation of semiconductor wafers: principles of ion beam scanning, dosimetry and uniformity control systems, charge neutralization and control, and machine and process parameters affecting throughput. Lastly, current state-of-the-art ion implantation systems and their performance will be presented.

Source Physics and Maintenance (Anthony (Tony) Renau)

This lecture examines the challenges and design requirements for ion sources and extraction systems that are used for ion implantation. The physics, functionality, and operation of ion sources will be discussed in some detail. The goals are to develop a good understanding of ion source design and operation, and to provide tips to maximize source life and optimize beam quality. The indirectly heated cathode source is described in some detail, along with some of its hot cathode predecessors. Some sources for special implant applications will also be described along with the features that make them well suited for those applications.

Safety Considerations in Ion Implantation (Ewald Wiltsche)

Ion implanters have several inherent hazards associated with their operation and maintenance. Although manufacturers of this equipment include numerous safety features into the design, the potential for serious injury or incident remains, particularly in situations where design safety features are overidden or recommended safe operating procedures are not followed. Although some incidences of equipment malfunction may, on their own, have the potential to result in a safety incident, these events are much more likely to occur during maintenance or service operations where personal interaction with the hazards of the equipment can be much more direct. Ion implanters have five main categories of hazard associated with them. These are hazardous materials, high voltage, radiation (ionizing and non-ionizing), mechanical systems, and ergonomic issues. In some instances, these categories can interact with each other to raise hazards that may not be readily recognizable to personnel. Specifics regarding each category and differences between operational and maintenance and service related issues will be discussed. Suggested safe operating procedures are also discussed.

Ion Beam Purity and Elemental Contamination (Michael Current)

Many factors related to the design, construction materials and operation of beamline and plasma systems can compromise the expected precision and cleanliness of the ion implantation process. In the last decade, the list of commonly used ions and target materials has greatly expanded beyond the classic set of Si dopants and wafers, greatly increasing the complications for beam purity. Among the issues to be discussed are: (1) “mass overlaps” resulting from various molecular ion breakup and change exchange events resulting from collisions with residual gases, (2) transport of energetic and vapor phase metals and dopants, (3) wetting of device structures by contaminant-containing atmospheric water vapor during load lock pump down and following cryo-implants, (4) organic materials contamination from vacuum oils, o-rings and implantation of resist out-gassing products, (5) particle transport, adhesion and ion blocking effects. Specific metrology methods, operational counter-measures and effects in nano-scale IC devices will be discussed for each contamination issue

Advanced Ion Implant Concepts (Leonard Rubin)

Ion implant applications continue to evolve to meet the needs of advanced devices. These devices include core logic, advanced memory, image sensors, and other specialty devices. This presentation will explain concepts in advanced devices, and new features in ion implant to address the needs of

these devices. The material will be divided into two parts. The first part will continue the discussion of the previous talk on logic devices, extending it to advanced memory and CMOS image sensors. The second part will discuss new implanter concepts applicable to all devices, particularly heated and cooled ion implantation.

Ion Implantation in Power Devices, new Base Materials and Solar Cells (Werner Schustereder)

Ion implantation processes contribute significantly to the development of power devices. In this case not smallest scale technologies according to Moore's law are addressed, but accurate treatment of the wafer frontside and backside structures as well as sometimes the bulk material itself play a crucial role to guarantee for key parameters such as highest power densities and minimal losses at required switching behavior. Some representative examples of the needs of high, medium and low power switching devices based on silicon technology are described and challenges for ion implantation processing are concluded. As of today the vast majority of power devices are fabricated on silicon substrates. However, other semiconductors like SiC and GaN obtain superior material characteristics compared to silicon. That is why considerable development effort is put into the understanding of how to fabricate devices based on those materials. One ingredient is the knowledge how ion implantation can affect and tailor their semiconductor properties. An overview on effects of ion implantation into these materials will be given. Additionally a short overview on the aspects of Ion Implantation for Silicon Solar Cells will be presented.

High Performance CMOS: 7 nm & Beyond (Devendra Sadana)

Despite soaring investment required to scale Si-CMOS technology beyond 5 nm nodes, Moore's law continues to thrive unabated! Although the current FinFET architecture is the likely candidate for the 5nm node, gate-all-around FETs with a nano-sheet (NS) architecture is fundamentally superior to the FinFET architecture for two reasons: (i) it provides higher drive current (I_{on} i.e., performance), and (ii) it achieves better device electrostatics (I_{off}, off current) which is ideal for low power applications. Further performance boost in the NS architecture is being explored with high mobility III-V channels especially when the supply voltage is scaled to < 0.5 V in future nodes. This talk discusses horizontally stacked gate-all-around (GAA) nanosheet (NS) technology in detail. It will be demonstrated that higher W_{eff} is inherent to the NS architecture which results in higher performance. Additionally, the NS technology allows for a simpler patterning scheme with EUV lithography which makes it attractive for high volume manufacturing. Excellent device electrostatics are shown even at L_g=12 nm despite aggressive 44 / 48 nm Contacted Poly Pitch (CPP) ground rules. It is further demonstrated that work function metal (WFM) replacement and multiple threshold voltages, compatible with aggressive sheet to sheet spacing for wide stacked sheets are possible with the NS technology.

Resumes of the Lecturers:

James Ziegler started **the *Ion Implantation Technology Conference*** in 1976 and the ***IIT School*** in 1982. He has done research in ion implantation since 1967, and helped to introduce the process into IBM's first manufacturing line for integrated circuits. He has written/edited 25 books in the field of ion beams and the effects of radiation on integrated circuits. He currently is a Professor at the United States Naval Academy in Annapolis, MD, USA.

Leonard Rubin received the S.B. degree in Materials Science and Engineering, and the S.M. and Ph.D. degrees in Electronic Materials from Massachusetts Institute of Technology. He worked at Zilog, Inc. in Nampa, Idaho on CMOS process integration in the areas of ion implantation, diffusion, and rapid thermal processing. He has been with Axcelis Technologies since 1995, where he is Chief Device Scientist. He has performed original research and development on advanced applications for high energy ion implantation, rapid thermal processing, and the effects of implant temperature and ion implant beam angle on advanced CMOS devices.

Michael Current has been active in the use of ion beams for doping, lamination and analysis of electronic materials for over 40 years and has been an instructor in the IIT school since 1982. After his PhD in Physics at RPI and 4 years on the research faculty at Cornell, he has worked as a process engineer, researcher and teacher in Silicon Valley, Texas, Japan and Taiwan for such companies as Signetics/Philips, XeroxPARC, Applied Materials, Frontier Semiconductor and a number of start-up operations. He was the founding president of the Silicon Valley Ion Implant Users Group in 1983 (now called the Junction Technology Group) and has taught implant and metrology courses at Kyoto U, Stanford, UC Berkeley, Santa Clara U. and Cheng Kung U. He has published over 240 papers and book chapters and is presently writing a textbook on implant process engineering.

Dick James graduated in 1971 with a Master's degree in Microelectronics and Semiconductor Devices from the University of Southampton in England. He has spent over 40 years working in the process development, design, manufacturing, packaging and reverse engineering of semiconductor devices. He worked with Chipworks (now TechInsights), an Ottawa, Canada-based specialty reverse engineering company, from 1995 to 2016 becoming their Senior Fellow/Technology Analyst, dealing with the microstructural characterization of devices, both process and package analyses. He is now Fellow Emeritus with TechInsights and a Senior Analyst with TechSearch International, based in Austin, a leading consulting company in the field of advanced semiconductor packaging technology.

Kevin S. Jones is the Chairman of the Department of Materials Science and Engineering at the University of Florida (Gainesville). He is co-Director of the Software & Analysis of Advanced Materials Processing Center (SWAMP). He has spent the past 20 years as a professor studying the processing induced defects in semiconductors. He has focused primarily on the area of transmission electron microscopy characterization of defects after ion implantation of various materials and developing an understanding of how defect evolution influences dopant diffusion. He has published over 300 papers on the field of ion implantation and is Chairman of the International Committee on Ion Implantation Technology.

Wilfried Lerch received a Diploma (1990) and a Ph.D. (1994) in physics from the Westfälische Wilhelms-University, Münster, Germany. Since 1994, he has been with AST Elektronik GmbH / Mattson Thermal Products GmbH Dornstadt, Germany, running the Technology Group. Since 2009 up to 2018 he has been the Director of Technology at centrotherm international AG, Blaubeuren, Germany, responsible for all kinds of thermal treatments (horizontal-, vertical-furnaces, RTP, low-temperature plasma oxidation and high temperature annealing for SiC and GaN). He has published over 100 papers in the field of rapid thermal annealing and ultra-shallow junction formation as well as a book on RTP technology and is a co-chairman of the German RTP user group.

Jiro Matsuo received Ph.D. degree in Electrical Engineering from Kyoto University. He is an associate professor of Graduate School of Engineering, Kyoto University. In 1984, he joined Fujitsu Co. to develop advanced CMOS devices and process. His research interests include ion beam process and characterization for advanced materials and devices. He served as deputy leader of "Cluster Ion Beam Technology" and "Advanced Quantum Beam Project" of MITI, in which collaborative research with many companies was carried out to develop industrial applications of cluster ion beam. He is now leading "Solid-Liquid Interface analysis with Cluster Ion Beam" project since 2014. He is expanding surface analysis techniques beyond high vacuum environment to near ambient pressure.

Bo Vanderberg received the B.Sc. in Mathematics and Physics at the Academy of Sciences in Strasbourg, France, and the M.Sc. in EE and Ph.D. in Industrial Electrotechnology at the Royal Institute of Technology in Stockholm, Sweden. He served as postdoctoral fellow at Uppsala University in Sweden, and was subsequently invited as visiting scientist to the Massachusetts Institute of Technology, and later Northeastern University, Boston. He then joined the staff of Axcelis Technologies, where he has been for the last 20 years, working on all aspects of ion implanter development. He is presently Technology Development Manager.

Anthony (Tony) Renau has held senior technical positions in the semiconductor industry for over 25 years, focusing mainly on ion implantation. He has been CTO at Varian Semiconductor since early 2003. Tony has a Ph.D. from the University of London. He has over forty publications and has given a number of invited and key note talks at various international conferences. He holds over thirty U.S. patents. Tony is on the international committee for ion implant technology, and now a member of Applied Materials Co.

Ewald Wiltsche is working on Ion Implanter Equipment for 27 years. Initially he started as a Maintenance Technician at Siemens Bauelemente OHG, stays now with Infineon Technologies since the beginning of this company in 1999. Within Infineon Technologies Ewald acts in various positions over the years mainly in the Ion Implantation Department and is responsible for radiation safety on Ion Implanters. Equipment Engineering on Ion Implanters and Laser Annealers is his main focus topic over the last 10 years. Various technical solutions for new innovations and Process Applications on Ion Implantation have successfully been developed with his major contribution. (e.g. 300mm Thin wafer Handling Method for Single Wafer Equipment and High efficient Sputter Ion Source for Mass Production) . Ewald is co-author of several patents. He sees the avoidance of work accidents and improvement of safety concerns on Ion Implanter Equipment as very important mission.

Werner Schustereder received the PhD degree in Ion Physics at the University of Innsbruck, Austria. After working at the Max Planck Institute for Plasma Physics in Munich on material science for nuclear fusion power plants he joined Infineon Technologies in 2008. Werner is responsible process development engineer in ion implantation and laser annealing at Infineon. He teaches courses on ion implantation, supervises diploma and PhD students and presents at international conferences on topics including mass spectrometry, nuclear fusion physics and defect engineering in semiconductors. Werner is co-author of ~60 peer-reviewed publications and several patents on methods for fabricating power devices. As a member of the steering group of the German Ion Implantation Users Group he is co-organizer of periodic knowledge exchange forums of the German-speaking implanter community.

Devendra Sadana has been with IBM Research at Yorktown Heights for last 31 years. Currently, he is a Distinguished Engineer at IBM Research and manages the advanced substrate research group. His latest research focuses on (i) developing optical communication and energy harvesting technologies for advanced IoT devices, (ii) engineering of SiGe and III-V channel materials for future COMS, and (iii) developing novel materials for neuromorphic devices. He has published over 300 papers in journals / conference proceedings, has written numerous review articles and book chapters. He is a co-inventor of over 500 issued patents and is included in the list of most prolific inventors in Wikipedia. He is a Fellow of SPIE.